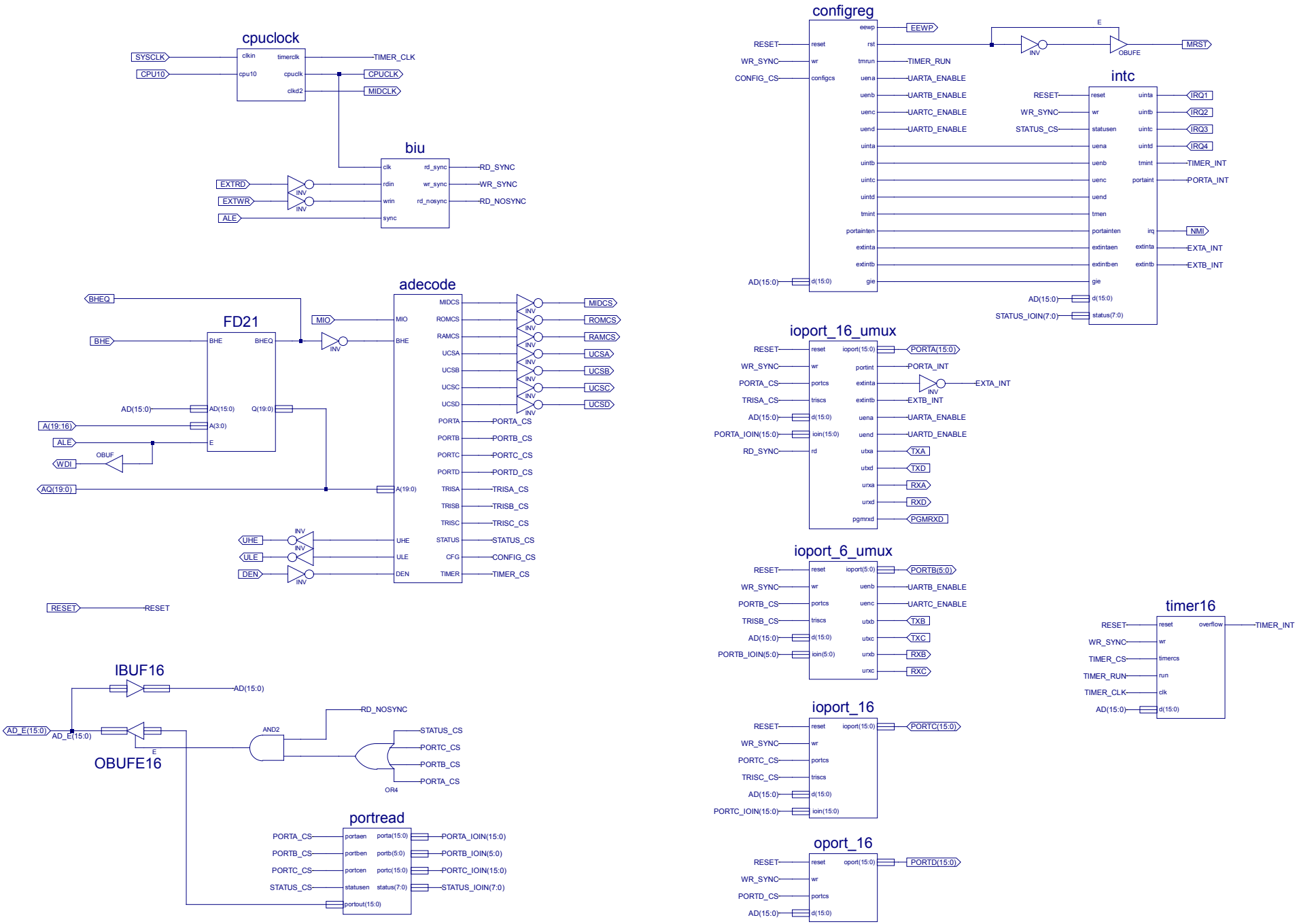
cpuclock
SYSCLK
CPU10
clkin
cpu10
timerclk
cpuclk
clkd2
TIMER_CLK
CPUCLK
MIDCLK
biu
EXTRD
EXTWR
ALE
INV
clk
rdin
wrin
sync
rd_sync
wr_sync
rd_nosync
RD_SYNC
WR_SYNC
RD_NOSYNC
adecode
BHEQ
BHE
FD21
MIO
AD(15:0)
A(19:16)
ALE
WDI
OBUF
AQ(19:0)
UHE
ULE
DEN
RESET
MIDCS
ROMCS
RAMCS
UCSA
UCSB
UCSC
UCSD
PORTA
PORTB
PORTC
PORTD
TRISA
TRISB
TRISC
STATUS
CFG
TIMER
PORTA_CS
PORTB_CS
PORTC_CS
PORTD_CS
TRISA_CS
TRISB_CS
TRISC_CS
STATUS_CS
CONFIG_CS
TIMER_CS
IBUF16
AD_E(15:0)
OBUFE16
E
AND2
OR4
portread
PORTA_CS
PORTB_CS
PORTC_CS
STATUS_CS
portaen
portben
portcen
statusen
portout(15:0)
porta(15:0)
portb(5:0)
portc(15:0)
status(7:0)
PORTA_IOIN(15:0)
PORTB_IOIN(5:0)
PORTC_IOIN(15:0)
STATUS_IOIN(7:0)
configreg
RESET
WR_SYNC
CONFIG_CS
reset
wr
configcs
d(15:0)
eewp
rst
tmrun
uena
uenb
uenc
uend
uinta
uintb
uintc
uintd
tmint
portainten
extinta
extintb
gie
EEWP
TIMER_RUN
UARTA_ENABLE
UARTB_ENABLE
UARTC_ENABLE
UARTD_ENABLE
OBUFE
MRST
intc
STATUS_CS
statusen
tmen
portainten
extintaen
extintben
status(7:0)
irq
IRQ1
IRQ2
IRQ3
IRQ4
TIMER_INT
PORTA_INT
NMI
EXTA_INT
EXTB_INT
ioport_16_umux
PORTA_CS
TRISA_CS
PORTA_IOIN(15:0)
RD_SYNC
portcs
triscs
ioin(15:0)
rd
ioport(15:0)
portint
utxa
utxd
urxa
urxd
pgmrxd
PORTA(15:0)
TXA
TXD
RXA
RXD
PGMRXD
ioport_6_umux
PORTB_CS
TRISB_CS
PORTB_IOIN(5:0)
ioin(5:0)
ioport(5:0)
utxb
utxc
urxb
urxc
PORTB(5:0)
TXB
TXC
RXB
RXC
ioport_16
PORTC_CS
TRISC_CS
PORTC_IOIN(15:0)
PORTC(15:0)
oport_16
PORTD_CS
oport(15:0)
PORTD(15:0)
timer16
TIMER_CS
TIMER_RUN
TIMER_CLK
timercs
run
clk
overflow